



INFORMATION DISCLOSURE
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| Application Number | 10/664,190 |
| Filing Date | September 16, 2003 |
| First Named Inventor: | Yervant Zorian et al. |
| Art Unit | 2138 |
| Examiner Name | Kerveros, James C. |
| Attorney Docket Number | 004640.P019 |

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| Sheet | 1 | of | 2 |
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U.S. PATENT DOCUMENTS

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| Examiner Signature | /James Kerveros/ (01/19/2007) | Date Considered | 01/19/2007 |
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| Sheet | 2 | of | 2 | Attorney Docket Number | 004640.P019 |
| NON PATENT LITERATURE DOCUMENTS | | | | | |
| Examiner Initials* | Cite No ¹ | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published | | | T ² |
| JK | ✓ | CHANG, Tsin-Yuan and ZORIAN, Yervant: "Tutorial 2: SoC Testing and P1500 Standard," Asian Test Symposium 2000: 492 | | | |
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| | ✓ | VARDANIAN, Valery A. and ZORIAN, Yervant: "A March-based Fault Location Algorithm for Static Random Access Memories," MDTD 2002: 256-261 | | | |
| ↓ | ✓ | BENSO, Alfredo, et. al., "HD-BIST: A Hierarchical Framework for BIST Scheduling and Diagnosis in SoCs," ITC 1999: 1038-1044 | | | |
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